

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Tu

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Patent No.:

6,853,024 B1

Serial No.:

10/679,098

Issue Date:

02/08/2005

Filed:

October 3, 2003

For:

Self-Aligned MIM Capacitor Process for Embedded DRAM

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Respectfully submitted,

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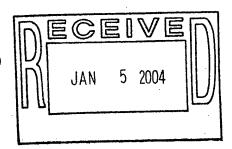


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10/679,098	10/03/2003	2811	770	TSM03-0188	17	19	3

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Applicant(s)

Kuo-Chi Tu, Hsin-Chu, TAIWAN;

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 12/30/2003

Projected Publication Date: 04/07/2005

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Early Publication Request: No

Title

Self-aligned MIM capacitor process for embedded DRAM

Preliminary Class

257

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January 5, 2005	(Date

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,098	10/03/2003	Kuo-Chi Tu	TSM03-0188	2276
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ITLE OF INVENTION: SELF-ALIGNED MIM CAPACITOR PROCESS FOR EMBEDDED DRAM

APPLN. TYPE	SMALL ENTITY	ISSUE FE	Е	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
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